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Strained GaN Quantum-Well FETs on Single Crystal Bulk AlN Substrates

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We report the first realization of molecular beam epitaxy grown strained GaN quantum well field-effect transistors on single-crystal bulk AlN substrates. The fabricated double heterostructure FETs exhibit a two-dimensional electron gas (2DEG) density in excess of $2\times10^{13}/\text{cm}^2$. Ohmic contacts to the 2DEG channel were formed by n^+ GaN MBE regrowth process, with a contact resistance of 0.13 Ω·mm. Raman spectroscopy using the quantum well as an optical marker reveals the strain in the quantum well, and strain relaxation in the regrown GaN contacts. A 65-nm-long rectangular-gate device showed a record high DC drain current drive of 2.0 A/mm and peak extrinsic transconductance of 250 mS/mm. Small-signal RF performance of the device achieved current gain cutoff frequency $f_T \sim 120$ GHz. The DC and RF performance demonstrate that bulk AlN substrates offer an attractive alternative platform for strained quantum well nitride transistors for future high-voltage and high-power microwave applications.

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State-of-art gallium nitride based electronic devices have demonstrated excellent performance in high-frequency and high-power applications[1–5]. These devices are on thick GaN buffer layers, most of which are on SiC substrates for efficient thermal dissipation. The heteroepitaxially grown GaN layers inherently incorporate high density of dislocations (typically $\sim 10^9/\text{cm}^2$), which give rise to reliability issues and degrade breakdown characteristics.

In this letter we show that thin strained GaN quantum well double heterostructures on bulk AlN substrates offer an attractive alternative approach for high-performance nitride electronics. To meet the scaling requirements for high-speed high-power RF applications, tight electrostatic control and quantum confinement of charge carriers are highly desired. The wide direct band gap of AlN (∼6.2 eV) and its large band offset with GaN offers the maximal vertical confinement of carriers in nitride channels. The large polarization charge of AlN induces high density two-dimensional electron gases (2DEG) in the quantum well, which is desired for high current drive and lateral scaling of gate lengths. The thermal conductivity of AlN, estimated[6] to be as high as ∼340 W/m·K can be comparable[7] to that of SiC ∼370 W/m·K, and offers the potential benefit of reducing thermal boundary resistance. Thus AlN simultaneously satisfies the conflicting requirements of high thermal conductivity and high electrical resistivity for high-power microwave electronics. Importantly, the low dislocation density ($\sim 10^4/\text{cm}^2$) of single-crystal bulk AlN substrates has the potential for defect-free channels and barriers in principle, which is a promising prospective for improving thermal robustness, reliability, breakdown, and noise characteristics of these devices[8]. The presence of a very thin GaN quantum well active region embedded in the AlN/GaN/AlN double heterostructure also enables selective optical-marker based Raman metrology of strain[9] present in the active layers.

We recently reported the transport properties and device performance of AlN/GaN/AlN heterostructures, but all those studies were performed on AlN templates on sapphire[10,11]. In that work, a number of fundamentally new design paradigms enabled by these heterostructures were outlined. In this letter we demonstrate the binary heterostructures on single crystal bulk AlN substrates. The DC and RF performance of the FETs on bulk AlN are improved from the counterparts on sapphire.

A schematic cross-section of the device structure is shown in Fig. 1 (a). The AlN/GaN/AlN heterostructures were grown by RF plasma molecular beam epitaxy (MBE) on ∼400 μm-thick semi-insulating Aluminum-polar bulk AlN substrates. Fig. 1 (b) shows the bulk AlN crystal. A 380-nm-thick unintentionally doped (UID) AlN buffer was epitaxially grown, followed by a 28 nm GaN quantum well where the 2DEG channel is located. Then, a 6-nm-thick AlN layer was grown on the GaN quantum well as the top barrier, and capped with a 1.5-nm-thick GaN layer to protect the AlN surface from oxidation. Hall effect measurements at room temperature showed a 2DEG density of $n_s \sim 2.8\times10^{13}/\text{cm}^2$, a room-temperature electron mobility of $\mu \sim 260$ cm^2/V·s, and a corresponding sheet resistance of $R_{sh} \sim 835$ Ω/□, with indications of defect generation during nucleation. This sample was used for subsequent HEMT fabrication. The mobility in such heterostructures can be significantly improved with modified nucleation conditions. For example, in a separate 3 nm AlN/ 21 nm GaN/ AlN quantum well heterostructure grown on the same bulk AlN substrate with different nucleation conditions, a 2DEG mobility of 601/1380 cm^2/V·s, a sheet charge density of $3.2/2.6\times10^{13}/\text{cm}^2$, and a sheet resistance of 327/171 Ω/□ at 300/77 K were observed. These are the highest measured mobility and lowest sheet resistance for the AlN/GaN/AlN strained quantum well heterostructures on the AlN platform till date. However the HEMT fabri-

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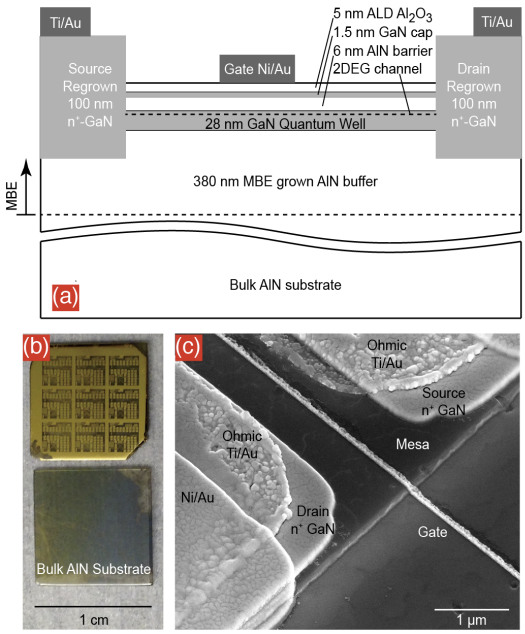

FIG. 1. (a) Schematic cross-section layer structure of the AlN/GaN/GaN heterostructure FETs on bulk AlN substrates (not to scale). (b) Images of a grown and processed sample (top), and an unprocessed bulk AlN substrate (bottom). (c) SEM image of a finished short gate length GaN quantum well field-effect transistor.

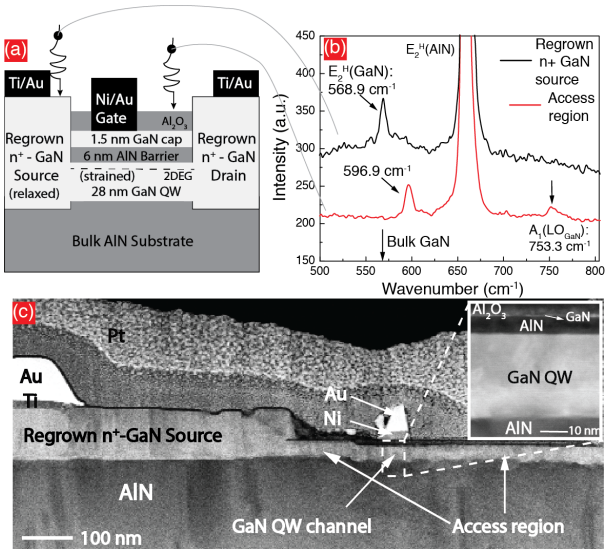

FIG. 2. (a) Schematic cross-section of the AlN/GaN/AlN FET consisting a 28-nm-thick GaN QW channel grown on bulk single-crystal AlN substrate. The measured locations by Raman spectroscopy are marked. (b) Raman spectroscopy as phonon probe measured for the access region, and the regrown source region. The Raman peak of the thick regrown GaN contact region is essentially identical to the bulk GaN peak shown by the arrow showing minimal residual strain. The thinner GaN QW channel in the access region is however significantly strained as indicated by the large shift in the peak. (c) $\mathcal{Z}$-contrast cross-section scanning transmission electron microscopy (STEM) image showing the structure of the FET in the dashed region in (a). The inset image shows the high resolution STEM of the gated GaN QW channel region.

cation process on this lower sheet resistance sample was not successful. At this stage, we do not completely understand the precise correlation between the nucleation conditions and the 2DEG transport properties. Several mechanisms could be limiting the Hall-effect mobilities in the strained QW channels, such as rough heterointerfaces, Stark-effect scattering[12], and hole-drag due to a co-existence of a two-dimensional hole gas (2DHG) channel at the bottom GaN/AlN interface[10]. A comprehensive study of transport is ongoing, and should help identify the lower measured electron mobilites in such heterostructures compared to 2DEGs on GaN substrates.

An MBE regrowth process was employed to form n+ GaN ohmic contacts to the 2DEG channel using a technique similar to what we have reported earlier[13–15]. A ∼200-nm-thick SiO_2 mask was deposited on the nitride heterostructures using plasma-enhanced chemical vapor deposition (PECVD) and then patterned by reactive ion etching (RIE). The nitride regrowth regions were etched for ∼40 nm using low-damage BCl_3/Cl_2 inductively coupled plasma reactive ion etching (ICP-RIE). MBE regrowth of ∼100-nm-thick heavily Si-doped ($N_D \sim 10^{20}/\mathrm{cm}^3$) n+ GaN was performed. The polycrystalline GaN deposited on the SiO_2 mask was lifted off selectively. Nonalloyed ohmic contacts were formed by E-beam evaporation of 20/100 nm Ti/Au stacks. Optical lithography was used to pattern and deposit 50/100 nm Ni/Au gates for long channel devices directly on the GaN cap layer as indicated in Fig 2(a), as well as on top of the Ti/Au layers as contacts. Before fabricating short gate length transistors, a 5 nm Al_2O_3 layer was deposited by atomic layer deposition (ALD) on the entire sample. Ni/Au (15/50 nm) gate stacks were defined by electron-beam lithography (EBL) and lift-off for short gate length devices on top of the ALD oxide, as indicated in Fig 1(a). A Scanning Electron Microscope (SEM) image of a finished device is shown in Fig. 1(c). The whole processed sample on the bulk AlN wafer is also shown in Fig. 1(b). Unlike Sapphire, the bulk AlN crystal is not completely transparent due to the presence of point defects.

The processed HEMT structure allowed the mapping of strain in the GaN quantum well channel using the optical marker technique[9]. Fig 2(a) indicates the locations where the Raman spectra shown in Fig 2(b) were measured. Fig 2(c) shows the source-side cross section of the processed device with a zoomed in image of the strained GaN quantum well under the gate. Because the regrown GaN regions are significantly thicker than the quantum well channel region, the difference in strain should be detectable in Raman spectroscopy. The measured E_2^H Raman peaks in the two regions shown in Fig 2(b), reveals the difference in the biaxial strain between these regions. The GaN quantum well region shows the expected peak

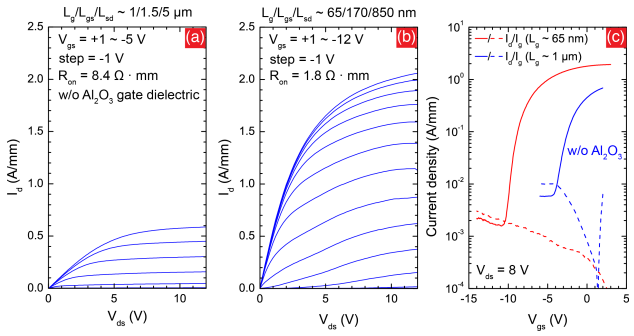

FIG. 3. DC common-source family of $I-V$s for (a) $L_g = 1$ μm and (b) $L_g = 65$ nm AlN/GaN/AlN FETs. (c) Transfer characteristics of both FETs in semi-log scale.

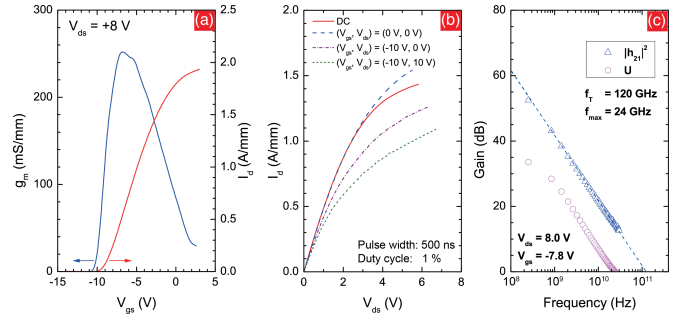

FIG. 4. (a) Transfer characteristics of the FETs with 65-nm-long gates in linear scale. (b) Pulsed IV measurements with a 500-ns pulse width and a 0.5-ms period. (c) Small-signal RF characteristics of the device showing current gain and unilateral gain f_T / f_{max} = 120/24 GHz.

at $E_2^H(QW) = 596.9$ cm^{-1}, indicating that the quantum well GaN is compressively strained. The peak frequency and the FWHM of the Raman peaks are similar to the epitaxial heterostructure before the FET device fabrication, indicating the FET device processing preserved the crystal quality in the thin GaN quantum well channel. The thicker n+ GaN regrown region shows a peak at E_2^H (n+ GaN) = 568.9 cm^{-1}, which is close to the bulk GaN peak of E_2^H (Bulk GaN) = 567.4 cm^{-1}. The small residual compressive strain ($< 0.2\%$) and high relaxation in the n+ regrown GaN regions is expected, because the thickness of 100 nm is large enough to relax the lattice mismatch almost completely in the heterostructure.

After the fabrication of the field-effect transistor, a 2DEG density of $n_s \sim 3.4 \times 10^{13}$/cm^2, an electron mobility of $\mu \sim 180$ cm^2/V·s, and a sheet resistance of $R_{sh} \sim 1020$ $\Omega/\square$ were extracted by Hall effect measurement at room temperature. The slight degradation from the as-grown sample may be due to the modification of surface states by the ALD Al_2O_3 layer. A contact resistance of 0.13 Ω·mm and a sheet resistance of 1100 $\Omega/\square$ were measured by an independent transmission-line method (TLM); the TLM sheet resistance was in good agreement with the the value obtained from the Hall effect measurement.

The measured DC common-source output characteristic current-voltage $I-V$'s of (a) a long channel FET and (b) a short channel AlN/GaN/AlN FET are shown in Fig. 3. The device dimensions are: (a) $W_g/L_g = 50/1\mu$m, $L_{gs}/L_{sd} = 1.5/5\mu$m, and (b) $W_g/L_g = 2 \times 50\mu$m/65 nm, $L_{gs}/L_{sd} = 170/850$ nm. At $V_{gs} = +1$ V and $V_{ds} = 12$ V, the maximum drain current density for the short channel FETs reaches $I_d^{max} \sim 2.0$ A/mm, which is ~3 times higher than the 0.6 A/mm measured for the long channel FETs. A 80-nm-long gate device exhibited drain current density of 2.8 A/mm at $V_{gs} = +3$ V and $V_{ds} = 12$ V. The reduction of the device dimensions thus dramatically boosts the current drive in spite of the high sheet resistance.

The current drive exceeding 2 A/mm is comparable to state-of-the-art GaN HEMTs on various other substrate platforms[1–5]. It is a significant improvement from the ~1.4 A/mm of the similar AlN/GaN/AlN FETs that were demonstrated earlier on an AlN-on-sapphire platform[10]. The on-resistance R_{on} was extracted to be ~ 8.4 Ω·mm and ~1.8 Ω·mm at $V_{gs} = +1$ V for long and short channel FETs, respectively. For the 65-nm-long gate devices, a high output conductance was observed for the 28-nm-thick GaN QW channel due to short-channel effects. With thinner GaN quantum wells and thinner gate barrier stacks, such short channel effects can be suppressed in the future by the presence of the AlN back barrier.

The on/off transfer characteristics of the long and short channel FETs are shown in Fig. 3(c) in a semi-log scale. The gate leakage current in the long-channel FET indicates that the MBE growth is not optimal yet, and defects have been generated in the epitaxial process. The ALD Al_2O_3 gate dielectric cuts down the leakage, improving the on/off ratio to three orders of magnitude for the short channel devices.

The linear plot of the transistor gain (transconductance) and the transfer characteristics of the 65-nm-long gate device are shown in Fig. 4(a) as a function of the gate voltage. The peak extrinsic transconductance reached is $g_m^{max} \sim 250$ mS/mm at $V_{gs} = -6.8$ V and $V_{ds} = 8$ V, corresponding to an intrinsic transconductance of 270 mS/mm for a source access resistance $R_s \sim 0.3$ Ω·mm. The threshold voltage V_{th} = -9.1 V at $V_{ds} = 8$ V was obtained by a linear extrapolation of the drain current at the peak transconductance. The negative threshold voltage is close to what is expected for the high 2DEG density (3.4×10^{13}/cm^2) and the gate capacitance.

The device performance under large-signal drive was investigated by pulsed $I-V$ measurements as shown in Fig. 4(b). Using 500-ns pulse width and a 0.5-ms period, the drain current density I_d at $V_{gs} = 0$ V cold pulsed from (V_{gs}, V_{ds}) = (0 V, 0 V) is observed to be higher than what is measured without pulsing at DC. The drain current drive pulsed from (-10 V, 0 V) and (-10 V, 10 V) showed a ~18% gate lag and a ~16% drain lag on the unpassivated devices. Current saturation is not observed

in the pulsed $I-V$ measurements due to short channel effects. To improve the large signal performance and enhance environmental robustness, passivation of surface states is necessary in future devices[16,17].

On-wafer device RF measurements were taken using an HP 8510C vector network analyzer in the frequency range from 0.25 to 30 GHz. Fig. 4(c) shows the current gain $|h_{21}|^2$ and the unilateral gain $\mathcal{U}$ as a function of the frequency for devices biased at peak f_T conditions (V_{gs} = -7.8 V, V_{ds} = 8.0 V). An unity current-gain cutoff frequency $f_T = 120$ GHz was extracted by the extrapolation of $|h_{21}|^2$ following the 20-dB/decade slope. Improving the mobility from the current value of ∼180 cm^2/V·s will reduce the channel charging delay and enable a higher f_T[18]. An $f_T \cdot L_g$ product of 7.8 GHz·μm was obtained, with for a gate-length-to-barrier-thickness aspect ratio of 5.2. For similar AlN/GaN/AlN FETs without a gate dielectric on AlN template on sapphire[10], the $f_T \cdot L_g$ product is 10.4 GHz·μm with aspect ratio of 13.3. Due to resistive rectangular gates, the measured low $f_{max} \sim 24$ GHz can be enhanced with T-gates[19] in future embodiments of the device.

In conclusion, this work reports DC and RF performance of AlN/GaN/AlN quantum well FETs on bulk AlN substrates with regrown ohmic contacts for the first time. By performing Raman spectroscopy with the AlN/GaN/AlN quantum wells as an optical marker, we demonstrate direct measurement of significant lateral strain variations between the GaN QW channel region and the regrown GaN region in the fabricated FET devices. With a 2DEG density of 3.4×10^{13}/cm^2, the devices pinched off and a record high drain current exceeding 2 A/mm was achieved. In spite of the low electron mobility, the 65-nm-long gate devices show an $f_T \sim 120$ GHz. As the homoepitaxial material quality improves, boosts in the electron mobility to the level in conventional GaN HEMTs (i.e. ∼1500 cm^2/V·s) is possible, which will result in a major boost in the performance of FETs on bulk AlN. The HEMT performance stands to benefit tremendously from the high thermal conductivity of the AlN substrate, and by improved lateral and vertical scaling afforded by the AlN substrate platform. By using thicker large bandgap AlN barrier layers and AlGaN channels, FETs on bulk AlN can significantly improve the breakdown characteristics and thermal handling over the existing state-of-the-art, and can present a compelling case for high power applications.

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